Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **BT**
2. **AT**
3. **FWD/REV**
4. **SA**
5. **SB**
6. **SC**
7. **OUTPUT ENABLE**
8. **REF OUT**
9. **CURRENT SENSE +INPUT**
10. **OSCILLATOR**
11. **ERROR AMP +INPUT**
12. **ERROR AMP -INPUT**
13. **ERROR AMP OUT/PWM INPUT**
14. **FAULT OUT**
15. **CURRENT SENSE -INPUT**
16. **GND**
17. **VCC**
18. **VC**
19. **CB**
20. **BB**
21. **AB**
22. **60°/N.120°**
23. **BRAKE**
24. **CT**

**.107”**

**.106”**

**3 2 1 24 23 22**

**21**

**20**

**19**

**18**

**17**

**16**

**16**

**9 10 11 12 13 14 15**

**4**

**5**

**6**

**7**

**8**

**08**

**-4**

**PWM**

**B**

**B35N**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 08 -4**

**APPROVED BY: DK DIE SIZE .106” X .107” DATE: 3/10/17**

**MFG: MOTOROLA THICKNESS .015” P/N: MC33035**

**DG 10.1.2**

#### Rev B, 7/1